Form PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR INFORMATION DISCLOSURE STATEMENT (Use Several Sheets if Necessary)	APPLICANT: David T. Blaauw et al.	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	ISSUE DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE (#43)	COUNTRY	CLASS	SUBCLASS
	AL					
	AM					
	AN					
	AO					
	AP					

OTHER INFORMATION (Including Author, Title, Date, Pertinent Pages, Etc.)

	AR	Burks et al., "Incorporating Signal Dependencies into Static Transistor-Level Delay Calculation," ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, pp. 110-119 (1997).
	AS	McDonald et al., "Computing Logic-Stage Delays Using Circuit Simulation and Symbolic Elmore Analysis," 38th Design Automation Conference Proceedings 2001 pp. 283-288.
	AT	Rao et al., "Eins TLT: Transistor Level Timing with Eins Timer," Proceedings from International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, IEEE Circuits and Systems Society, pp. 1-6 (1999).
	AU	
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